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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/586,800

07/19/2006

Yongxiang Han

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01/21/2009

INTEL/BSTZ

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EXAMINER

YU, JAE UN

ART UNIT

PAPER NUMBER

2185

MAIL DATE

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/586,800	Applicant(s) HAN ET AL.	
	Examiner JAE U. YU	Art Unit 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12/30/08.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

The examiner acknowledges the applicant's submission of an amendment dated 12/30/2008. At this point, claims 2, 3, 7, 8, 9, 14, 19 and 20 have been amended. Thus, claims 1-22 are pending in the instant application.

Response to Amendment

In view of the applicant's amendment, the 35 USC 112 rejection for claim 14 is withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-4, 7-12, 14-16 and 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Chatterjee et al. (US 2005/01829906), referred to as "Chatterjee" hereinafter.

2. As per independent claims 1, 9 and 14 & dependent claim 3 and 20, Chatterjee discloses; "updating an entry in a memory [**updating the cache memory in**

the first controller, Paragraph 12] external to the network processor”, “identifying a microengine of the plurality of microengines that has stored the entry in a local memory **[“mirrored cache memory” of the peer controller, Paragraph 12]** for the microengine”, and “writing information to a scratch ring of a buffer for the identified microengine that indicates the entry has been updated **[buffering update information, Paragraph 12]**”.

3. As per **independent claim 19 & dependent claims 2 and 10**, Chatterjee discloses; “a machine readable medium comprising a plurality of instructions that in response to being executed result in a network device **[programmed instructions executed on a general or special purpose processor, Paragraph 87]**”, “updating an entry in a memory **[updating the cache memory in the first controller, Paragraph 12]** external to a network processor of the network device”, “identifying each microengine of the network processor that has cached the entry in a local memory of the network processor **[“mirrored cache memory” of the peer controller, Paragraph 12]**”, “storing information to a corresponding buffer for each identified microengine, the information indicating the entry has been updated in the memory external to the network processor **[buffering update information, Paragraph 12]**”, and “reading the entry from the external memory to the network process to update the entry cached in the local memory based upon the information in the corresponding buffer for each identified microengine **[updating the mirrored cache memory of the peer controller based upon the information in the buffer, Paragraph 12]**”.

4. As per **claims 11, 15**, Chatterjee discloses; “reading the entry from the memory external to the network processor in response to determining, based upon the information written to the buffer **[buffering update information, Paragraph 12]**, that the entry has been updated”, and “updating the local memory for the microengine based upon the entry read from the memory external to the network processor **[transmitting associated cache data from the first controller, Paragraph 12]**”.

5. As per **claims 4, 12, 16 and 21**, Chatterjee discloses; “updating the entry in the local memory for the microengine in response to determining, based upon the information written to the buffer **[updating the mirrored cache memory of the peer controller based upon the information in the buffer, Paragraph 12]**, that the entry has been updated”, and “processing a network packet based upon the entry based in the local memory for the microengine”.

6. As per **claim 7**, Chatterjee discloses; “wherein the information further indicates that all entries in the local memory for the microengine are invalid, if more than a threshold number of entries of the memory external to the network processor are updated **[buffering update (“invalid”) information, Paragraph 12]**”.

7. As per **claim 8**, Chatterjee discloses; “flushing all entries in the local memory for the microengine **[updating the “peer controller” (update requires flushing old**

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data), Figure 2] in response to information stored in the buffer for the microengine **[buffered update information, Paragraph 12]**".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 5, 6, 13, 17, 18 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chatterjee et al. (US 2005/01829906) in view of Joy et al. (US 2002/0138717), referred to as "Joy" hereinafter.
2. As per claims 5, 6, 13, 17, 18 and 22, Chatterjee discloses; "update entries of a corresponding local memory for each microengine based upon information stored in a corresponding buffer for each microengine **[updating the mirrored cache memory of the peer controller based upon the information in the buffer, Paragraph 12]**".

Chatterjee does not disclose expressly the "plurality of threads".

Joy discloses a multithread system in the abstract.

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Chatterjee and Joy are analogous art because they are from the same field of endeavor of data processing system.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Chatterjee by implementing the multithread system as taught by Joy in the abstract.

The motivation for doing so would have been increased parallelism as expressly taught by Joy in paragraphs 10 and 16.

Arguments Concerning Prior Art Rejections

1st Point of Argument

Regarding claim 1, the applicant argues that Chatterjee fails to teach the limitations of "identifying a microengine of the plurality of the microengines" and "writing information to a buffer for the identified microengine". However, Chatterjee discloses a "peer controller" in paragraph 12 that corresponds to the claimed "microengine", and further discloses buffering update information for the "peer controller" in paragraph 12. Further, the applicant argues that Chatterjee fails to teach "a network processor". However, Chatterjee discloses a network device implementation in paragraph 30. The examiner notes that the "mirrored cache memory" corresponds to the claimed "local memory".

2nd Point of Argument

Regarding claim 2, the applicant argues that Chatterjee fails to teach the claimed limitations. However, Chatterjee clearly teaches reading the entry from the first controller to update the peer controller based upon the update information written to the buffer in paragraph 12.

3rd Point of Argument

Regarding claim 3, the applicant argues that Chatterjee fails to teach a “scratch ring” of the buffer. However, a generic term such as “a scratch ring” does not represent a patentable distinct feature, and should be more thoroughly defined in the claim.

4th Point of Argument

Regarding claim 7, the applicant argues that Chatterjee fails to teach the claimed limitation. However, Chatterjee discloses buffered update information in paragraph 12, which indicates that the entries are “invalid”, wherein such operation occurs in response to each update. Thus, Chatterjee teaches a threshold of zero.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

A. Claims Rejected in the Application

Claims 1-22 have received a second action on the merits and are subject of a second action final.

B. Direction of Future Remarks

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submission should be clearly labeled "Comments on Statement of Reasons for allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae Un Yu who is normally available from 9:00 A.M. to 5:30 P.M. Monday thru Friday and can be reached at the following telephone number: (571) 272-1133.

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If attempts to reach the above noted examiner by telephone are unsuccessful, the Examiner's supervisor, Sanjiv Shah, can be reached at the following telephone number: (571) 272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jae U Yu/

Examiner, Art Unit 2185

1/17/2009

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185